In the Claims:

Please amend claims 1 and 20. The claims are as follows:

1. (CURRENTLY AMENDED) An electronic structure comprising:

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a top surface that includes a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a mass of a single conductive material, wherein a first portion of the mass forms ~~forming~~ ~~a~~ an external layer upon the selected area of the top surface of the second metal layer such that the external layer is external to the microvia cavity and external to the substrate, and wherein a second portion of the mass totally fills ~~and totally filling~~ the microvia cavity and ~~being~~ is in contact with the first contact area of the first metal layer.

2. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the mass of the single conductive material conformally fills the microvia cavity.

3. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the mass of the single conductive material has a planar surface forming a contact pad located parallel to and opposite the first contact area of the first metal layer.

4. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein selected area is approximately centered around the first contact area.

5. (PREVIOUSLY PRESENTED) The structure of claim 4, wherein the second metal layer within the selected area is approximately centered around the microvia cavity.

6. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the second metal layer within the selected area is approximately centered around the first contact area.

7. (ORIGINAL) The structure of claim 1, wherein the second metal layer contains a flat copper ring around the microvia cavity.

8. (ORIGINAL) The structure of claim 1, wherein the microvia cavity includes a truncated cone-shaped hole in the dielectric layer.

9. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the mass of the single conductive material comprises at least one of a solder paste, a reflowable solder, a conductive paste, and a conductive adhesive.

10-19. (CANCELED)

20. (CURRENTLY AMENDED) An assembly comprising:

a semiconductor chip;

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a top surface that includes a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a continuous mass of a single conductive material, wherein a first portion of the mass forms ~~forming a~~ an external layer upon the selected area of the top surface of the second metal layer such that the external layer is external to the microvia cavity and external to the substrate, wherein a second portion of the mass totally fills ~~and totally filling~~ the microvia cavity and ~~being~~ is in contact with the first contact area of the first metal layer, and wherein the semiconductor chip is electrically connected to the mass of the single conductive material.

21. (PREVIOUSLY PRESENTED) The assembly of claim 20, wherein the selected area is a planar area.

22. (PREVIOUSLY PRESENTED) The assembly of claim 20, wherein the selected area is a planar area that is about parallel to a planar top surface of the first metal layer.

23. (PREVIOUSLY PRESENTED) The assembly of claim 20, wherein an etch rate of the single conductive material is less than an etch rate of a metal comprised by the second metal layer.

24. (PREVIOUSLY PRESENTED) The assembly of claim 20, wherein the single conductive material is bondable to a wall of the microvia cavity.

25. (PREVIOUSLY PRESENTED) An assembly comprising:

a semiconductor chip;

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a top surface that includes a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a mass of a single conductive material forming a layer upon the selected area of the top surface of the second metal layer and totally filling the microvia cavity and being in contact with the first contact area of the first metal layer, wherein the semiconductor chip is electrically connected to the mass of the single conductive material, wherein the single conductive material is not bondable to a wall of the microvia cavity.

26. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the selected area is a planar area.

27. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the selected area is a planar area that is about parallel to a planar top surface of the first metal layer.

28. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein an etch rate of the single conductive material is less than an etch rate of a metal comprised by the second metal layer.

29. (PREVIOUSLY PRESENTED) The structure of claim 1, wherein the single conductive material is bondable to a wall of the microvia cavity.

30. (PREVIOUSLY PRESENTED) An electronic structure comprising:

a substrate having a dielectric layer between a first metal layer and a second metal layer, the second metal layer being disposed above the first metal layer, the first metal layer having a first contact area, the second metal layer having a top surface that includes a selected area disposed above the first contact area;

a microvia cavity within the selected area being disposed through the second metal layer and through the dielectric layer and extending to the first contact area of the first metal layer; and

a mass of a single conductive material forming a layer upon the selected area of the top surface of the second metal layer and totally filling the microvia cavity and being in contact with the first contact area of the first metal layer, wherein the single conductive material is not bondable to a wall of the microvia cavity.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and credit Deposit Account No. 09-0457 (IBM).

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